AN OVERVIEW OF HARDWARE ISSUES FOR IP AND ATM

“Name one thing you could achieve with ATM that you couldn’t with IP!”

Nick McKeown
Assistant Professor of Electrical Engineering and Computer Science
Stanford University
nickm@ee.stanford.edu
http://ee.stanford.edu/~nickm

Outline

Part I
- The need
- Trends in ATM switches
- Trends in IP routers
- Merging of the two

Part II
- Some key technologies
- Summary

What’s the Problem?

Most things

Time

The demand

The San Jose NAP

Source: http://www.mfdata.net/MAE/west.stats.html

2/25: Merging IP and ATM

3/25: Merging IP and ATM

4/25: Merging IP and ATM
The supply

Why we need faster routers

The race is on...

Trends in ATM switches

- Ascend (Netstar), Ipsilon, Toshiba, BBN, [Cisco, Bay, Juniper, Torrent] ?........
Trends in IP routers

Generic IP Router:

Merging of IP & ATM

Merging of IP & ATM

Most routers do this poorly!

Trend 1: Move CPU off forwarding path

Most routers today use caching
**Trends in IP routers**

**Trend 2: AVOID SHARED BUS**

1. LINE → CPU
2. LINE → CPU

**Consequence**

1. ROUTER
2. VCXT
3. VCXT
4. VCXT

**IP Switching**

**Tag Switching**

**The fundamental hardware difference between IP & ATM**

- **VCI**: 24 bits, 1 entry per active flow, 32-64K entries
- **IP DA**: 32 bits, 1 entry per dest. subnet, 50-100K entries

**Claim**

If we could do FAST longest prefix matches

Then we wouldn’t be here!

**BUT:**

ATM VCI ≈ 16 bits AND we get to choose!
Merging of IP & ATM

Why?

If you could get the whole IP forwarding table in fast memory (and update it invisibly!) then who needs ATM?

Removing IP forwarding engine from the datapath is one thing: but still need Quality Processor on the critical path.

Large number of individual flows (ISMP Flow Type 1)
=> aggregation onto coarser src-dest flows (Type 2)
=> need reassembly/frame-mode switches

Some key hardware technologies

- Memory bandwidth
- Serial link technology

- Special-purpose memories
- CPU vs special-purpose processors

Memory Bandwidth

![Memory Speed vs Time Graph]

- SRAM
- DRAM

Output queueing running out of steam!

Trends in ATM switches

How fast can this architecture go?

![5ns SRAM Shared Memory]

How fast can a 16 port switch operate with this architecture?

• cell per port
Serial link technology

“wires are becoming a scarce resource”

Standard interfaces are a bottleneck:
- 100 Mbit/sec per pin is tough.
- 100 signal pins for 10 Gbit/sec.
- Large chip packages and board connectors drive up costs.

Serial interfaces are efficient:
- 1 Gbit/sec per pin.
- 10 signal pins for 10 Gbit/sec.

Problems with High Speed Links

- Precise timing needed
  - Hard to determine which bit is which.
  - Distributed clocks have skew (1 ns/bit time at 1 Gb/s).
  - Solution: recover timing from data.

- High speed signals
  - Need to transmit and receive 1 Gb/s.
  - Solutions: low swing signals, good terminations on transmission lines.

Much ongoing R&D in this area.

Special purpose memories

1. FIFOs

2. Programmable FIFOs

CPU vs. special-purpose processor

1. Cache Interface

2. Packets

   Forwarding Tables
e.g. BayBridge
Summary

- **Trends in switching**
  - Single-stage shared memory and busses are running out of steam.
  - Combined I/O Queueing and/or multistage switches are required.

- **Trends in routing**
  - Removal of CPUs from forwarding path.
  - Quality Processor still on the main forwarding path.

- **Key Technologies**
  - Memory Bandwidth
  - Serial link technology
  - Special-purpose memory
  - Special-purpose processors